MPC9893/MPC9993/MPC9894

Intelligent Dynamic Clock Driver Family

A new class of clock drivers offer a one chip clock generation and switching solution increasing reliability in computing, networking and telecommunication systems.

Meeting the demand for the most critical requirements in high performance computing, networking and telecommunication applications, the integrated Intelligent Dynamic Clock Switch (IDCS) family continuously monitors both clock input signals and indicates a clock failure individually for each clock input. When a false clock signal is detected, the failover clock will switch over to the redundant clock input, forcing the phase lock loop (PLL) to slowly slew to alignment with near zero delay capabilities.

MPC9893: Low Voltage Intelligent Dynamic Clock Switch

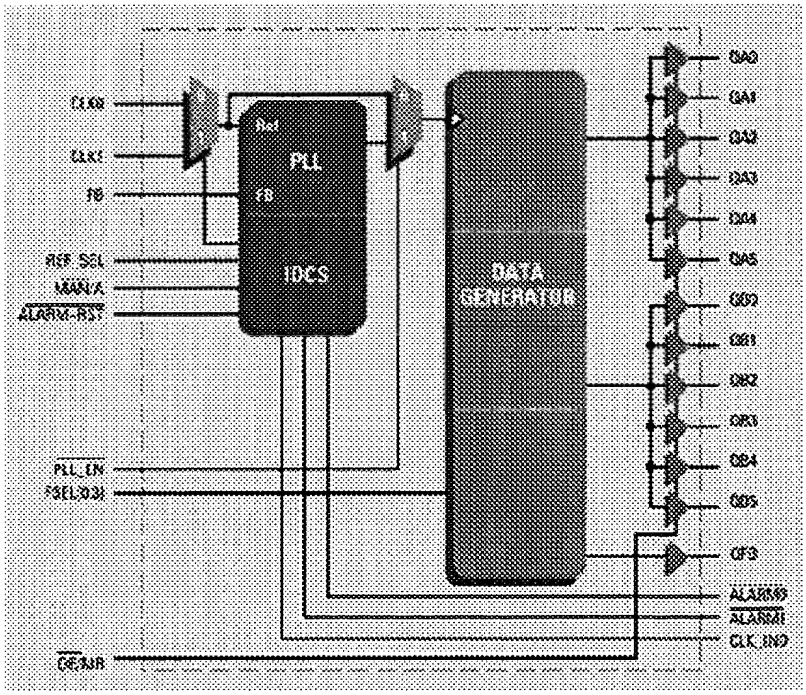
The MPC9893 is a 2.5V or 3.3V compatible PLL clock driver and clock generator. The clock generator uses a fully integrated PLL to generate clock signals from redundant clock sources. The PLL multiplies the input reference clock signal by one, two, three, four or eight. The frequency-multiplied clock drives six bank A outputs. Six bank B outputs can run at either the same frequency or at half of the bank A frequency. Therefore, bank B outputs additionally supports the frequency multiplication of the input reference clock by 3? and 1?. Bank A and bank B outputs are phase-aligned. Due to the external PLL feedback, the clock signals of both output banks are also phase-aligned to the selected input reference clock, providing virtually zero-delay capability.

The MPC9893 also provides a manual mode that allows for user-controlled clock switches. The PLL bypass of the MPC9893 disables the IDCS and PLL-related specifications do not apply. In PLL bypass mode, the MPC9893 is fully static in order to distribute low-frequency clocks for system test and diagnosis. Outputs of the MPC9893 can be disabled

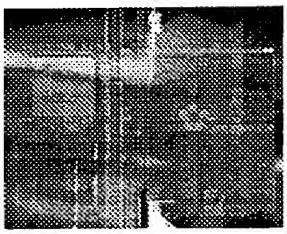
(high-impedance tristate) to isolate the device from the system.

MPC9893 Features

- 12 output LVCMOS PLL clock generator
- 2.5V and 3.3V compatible
- 6.25 - 200 MHz output frequency range
- Ambient operating temperature range of -40蚓 to +85 蚓
- Low skew characteristics: maximum 150 ps output-to-output (within bank)
- Automatically detects clock failure
- Smooth output phase transition during clock failover switch
- LVCMOS compatible inputs and outputs
- External feedback enables zero-delay configurations
- Output enable/disable and static test mode (PLL bypass)
- Supports networking, telecommunications and computer applications
- 48 lead LQFP package



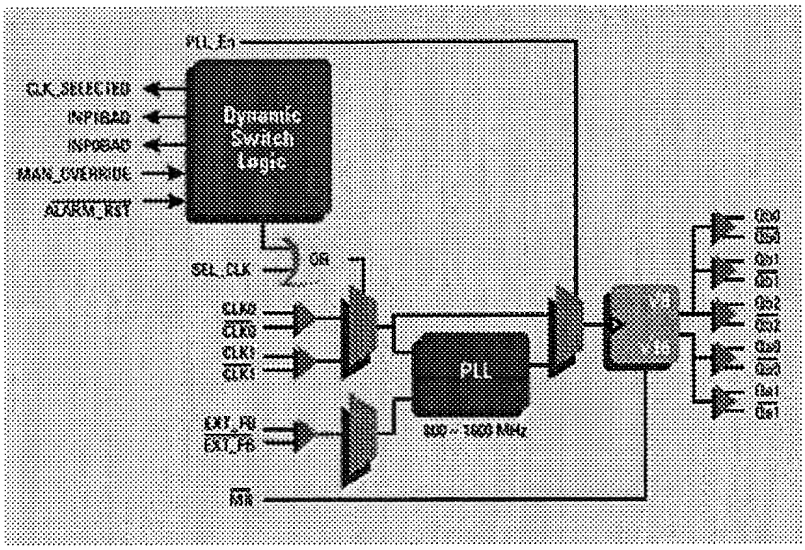
MPC9993: Intelligent Dynamic Clock Switch
The MPC9993 Intelligent Dynamic Clock Switch (IDCS) circuit continuously monitors both input clock signals. Upon detection of a failure (clock stuck HIGH or LOW for at least 1 period), the INP_BAD for that clock will be latched (H). If that clock is the primary clock, the IDCS will switch to the good secondary clock and phase/frequency alignment will



occur with minimal output phase disturbance. The typical phase bump caused by a failed clock is eliminated.

MPC9993 Features

- Fully integrated PLL
- Intelligent dynamic clock switch
- LVPECL clock outputs
- LVCMOS control I/O
- 3.3V operation
- 32-lead LQFP Packaging
- SiGe technology supports near-zero output skew
- Ambient temperature range -40蚓 to +85蚓
- Pin and function compatible to the MPC993



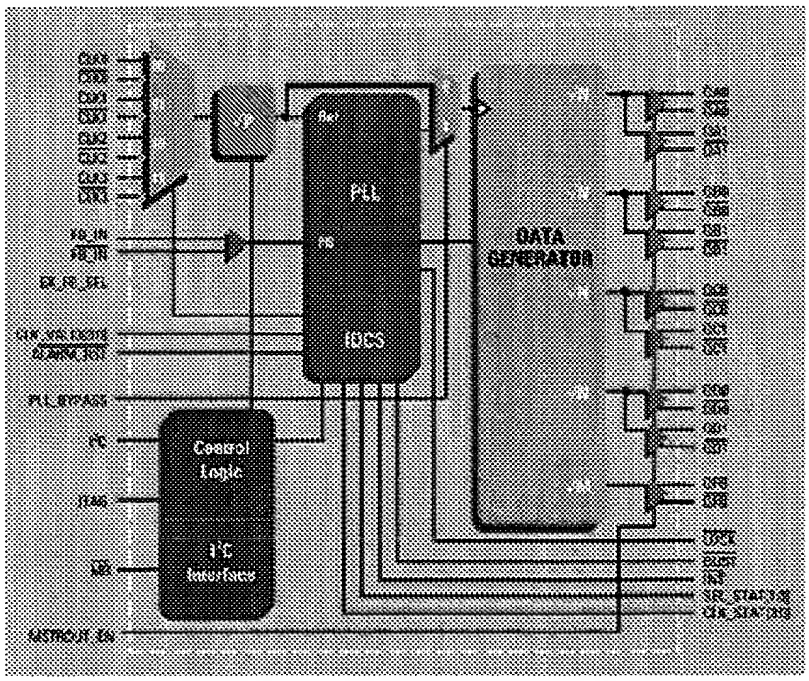
MPC9894: Redundant Clock Generator and Fanout Buffer with Redundant Inputs

The MPC9894 is quad input redundant differential clock generator. The device contains logic for clock failure detection and auto switching for clock redundant applications. The generator uses a fully integrated PLL to generate clock signals from up to four redundant clock sources. The PLL multiplies the frequency of the input reference clock by one, two, four, eight or divides the reference clock by two or four. The frequency-multiplied clock signal drives four bank of two differential outputs, each bank allows an individual frequency-divider configuration. All outputs are phase-aligned and due to the external PLL feedback, the clock signals of all output are also phase-aligned to the selected input reference clock, providing virtually zero-delay capability.

MPC9894 Features

- 8 output differential LVPECL PLL clock generator

- Ambient operating temperature range of -40蚓 to +85 蚓
- 3.3 supports 2.5 or 3.3V supplies with 2.5V and 3.3V I/O
- 27.5?40MHz output frequency range
- Low skew characteristics: 50ps1 output-to-output
- Quad redundancy reference inputs
- Smooth output phase transition during clock failover switch
- Clock activity monitor
- Clock qualifier inputs
- Manual clock select and automatic switch modes
- Specified frequency and phase slew rate on clock switch
- LVCMOS compatible control inputs and outputs
- JTAG Interface
- External feedback enables zero-delay configurations
- I2C interface for device configuration
- Designed for computing, networking and telecommunications applications
- 100 pin MAPBGA package, 11x11mm



MPC9893/D, MPC9894/D and MPC9993/D data sheets and block diagrams are available at:
www.motorola.com/AdvancedClockDrivers

Contact Information
Motorola offers user's manuals, application notes and sample code for all of its communications processors. In addition, local support for these products is also provided.

This information can be found at:
http://motorola.com/smartnetworks/

For all other inquiries on Motorola products contact the Customer Response Center at: 800-521-6274 or www.motorola.com/semiconductors

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